REMARKS

Claims 81-85 and 90-93 are pending in the present application. In the Office Action dated December 22, 2003, the Examiner rejected claims 85 and 90 under 35 U.S.C. 102(b) as being anticipated by an IBM Technical Disclosure Bulletin, "Decoupling Capacitor Structure to Reduce FET Output Driver Switching Noise", December 1, 1987, page 167-168 ("IBM-87"). Additionally, the Examiner rejected claims 85 and 93 under 35 U.S.C. 102(b) as being anticipated by an IBM Technical Bulletin, "Clipped Decoupled Twin-Carrier Module for IC Memory Chips", January 1, 1985, page number 4857-4858 ("IBM-85"). Further, claims 81-85 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,027,253 to Lauffer *et al.* ("Lauffer"). The Examiner has also objected to the drawings as failing to comply with 37 CFR 1.84 (p)(5) because they include reference signs not mentioned in the description. Additionally, the Examiner rejected claims 81-85 and 90-93 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. The Examiner has further pointed out that the applicants have not filed a copy of the priority application as required by 35 U.S.C. 119(b). Please note that the applicants are complying with this requirement by including with this Amendment a Certified Copy of the United Kingdom Priority Application No. 0126821.8. Applicants disagree with these rejections and wish to clarify various distinctions of applicants' invention over the cited art. Reconsideration of the invention is therefore requested in light of the following remarks.

In the remarks that follow, various technical differences between the references cited by the Examiner and the embodiments of the present invention are discussed. It is understood, however, that any discussion involving various embodiments of the invention, which are disclosed in detail in the applicants' specification, do not define the scope or interpretation of any of the claims. Moreover, any discussion of differences between the references cited and the various embodiments of the invention are intended only to help the Examiner to appreciate the importance of the claimed distinctions as they are discussed.

The various embodiments of the present invention are directed to methods and apparatuses for conductively isolating individual electronic modules positioned within an electronic package assembly. It is often desirable to provide conductive isolation of the type

disclosed in the present application in order to properly configure a networking system. For example, IEEE 1394 specifies that all devices coupled to a serial bus must have the same reference ground potential as provided by a ground wire of the serial bus. It is widely known, however, that separate devices coupled to the bus may have different ground potentials. Such voltage differences may result in a direct current flowing from a device having the higher potential to a device having the lower potential. Such currents are recognized to have undesired effects, including signal degradation and may even result in physical damage to the devices. Thus, it is desirable that a ground wire of the serial bus be conductively isolated from other devices on the bus so that selected devices coupled to the serial bus operate on the same isolated ground domain.

Accordingly, in a pertinent embodiment of the invention, as shown in Figure 3 of the present application, a first module 304 and a second module 305 are positioned on a supporting substrate 302. A ground plane of the first module 304 is conductively coupled to a first conductive surface 310, and a ground plane of the second module 305 is coupled to a second conductive surface 312 by various well-known methods, including wire bonding. The first conductive surface 310 and the second conductive surface 312 are spaced apart relative to one another, and have a dielectric material 314 positioned between the first layer 310 and the second layer 312. The first conductive surface 310 and the second conductive surface 312 thus cooperatively form a capacitor so that the respective ground planes of the modules 304 and 305 are capacitively coupled so that direct currents are effectively blocked.

The Examiner has cited IBM-87 for disclosing a decoupling capacitor within an electronic module having a first module (as disclosed in the reference, a field effect transistor) and a second module (as disclosed, a field effect transistor module), wherein the decoupling capacitor is coupled between the first module and the second module. Applicants note that the cited reference fails to disclose or fairly suggest a first conductive surface coupled to a ground plane of the first module and a second conductive surface coupled to a ground plane of a second module, wherein the first ground plane and the second ground plane are spaced apart by a dielectric.

The examiner has also cited the IBM-85 reference. IBM-85 discloses a twin carrier module having a supply voltage decoupling capacitor positioned between a pair of

opposing chip carriers. IBM –85 does not disclose or fairly suggest a first conductive surface coupled to a ground plane of the first module and a second conductive surface coupled to a ground plane of a second module, wherein the first ground plane and the second ground plane are spaced apart by a dielectric.

Finally, the Examiner has cited the Lauffer reference. Lauffer discloses a multiplayer circuit package having a buried thin film capacitor positioned in the structure. Lauffer does not disclose or fairly suggest a first conductive surface coupled to a ground plane of the first module and a second conductive surface coupled to a ground plane of a second module, wherein the first ground plane and the second ground plane are spaced apart by a dielectric. If the undersigned has missed a relevant teaching in the Lauffer reference, the Examiner is kindly requested to point out where this teaching may be found.

Turning now to the claims, specific differences between the claim language and the applied art will be pointed out. Claim 81, as amended, recites in pertinent part: "A method of *conductively* isolating modules within an integrated circuit package assembly, comprising...attaching a first and second module to a substrate having a first and opposing second side...providing a first conductive surface having a first and opposing second side abutting the opposing second side of the substrate...providing a dielectric layer having a first and opposing second side abutting the opposing second side of the first conductive surface...providing a second conductive surface abutting the opposing second side of the dielectric...*conductively coupling the first conductive surface to a ground plane of the first module*...and...*conductively coupling the second conductive surface to a ground plane of the second module.*" (Emphasis added). The applied references do not disclose or fairly suggest this. Accordingly, claim 81 is now allowable over the cited art. Claims depending from claim 81 are also allowable based upon the allowable form of the base claim and further in view of the additional limitations recited in the dependent claims.

Claim 85, as amended, recites in pertinent part: "A method of *conductively* isolating modules within an integrated circuit package assembly, comprising...forming a capacitor within the semiconductor package assembly, the capacitor having a first terminal and a second terminal...*coupling a ground plane of a first module to the first terminal of the capacitor*...and...*coupling a ground plane of a second module to the second terminal of the*

capacitor." (Emphasis added). Again, none of the applied references, either singly or in combination disclose or suggest this. Therefore, claim 85 is now allowable over the cited art. Claims depending from claim 85 are also allowable based upon the allowable form of the base claim and further in view of the additional limitations recited in the dependent claims.

Applicants have amended the specification thereby placing the drawings in compliance with 37 C.F.R. § 1.84(p)(5).

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP

Steven H. Arterberry
Registration No. 46,314
Telephone No. (206) 903-8787

SHA:tlm

Enclosures:
Postcard
Fee Transmittal Sheet (+ copy)
Certified Copy of United Kingdom Priority Application No. 0126821.8

DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101-4010
(206) 903-8800 (telephone)
(206) 903-8820 (fax)

h:\ip\documents\clients\micron technology\900\500986.02\500986.02 amend oa 122203.doc